PATENT ABSTRACTS OF JAPAN

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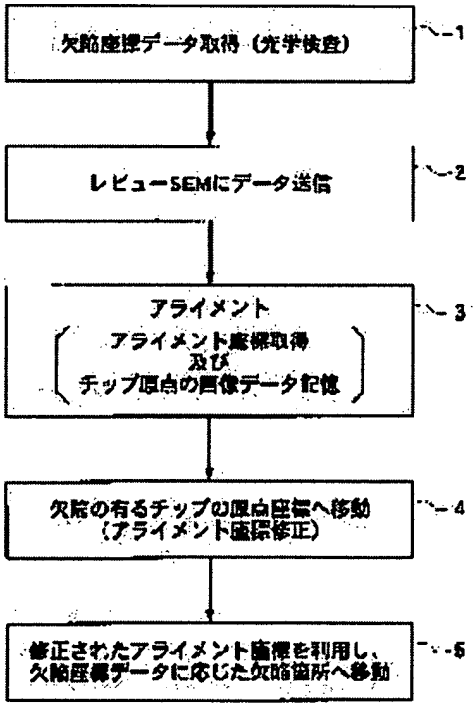
(54) METHOD FOR RECOGNIZING WAFER COORDINATE OF AUTOMATIC DEFECT DETECTOR

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a method for recognizing a wafer coordinate of an automatic defects detector capable of enhancing coordinate precision and obtaining accurately a defective recognition image with high magnification.

SOLUTION: The automatic defect detector extracts actual defective portions on a wafer under test as an image by means of a review SEM in reference to defective coordinate data obtained from the wafer. In step 3, an arbitrary image data in a point of origin of a chip are stored when a coordinate data is incorporated to obtain an alignment coordinate with respect to the wafer under test. In step 4, difference in the alignment coordinate is corrected by temporarily shifting the image data in the point of origin of the chip to origin coordinate of the defective chip in reference to the defective coordinate data to be superposed with each other. Thereafter, the image data is transferred to the defective portion corresponding to the defective coordinate data obtained in step 1 on the basis of the corrected alignment coordinate.



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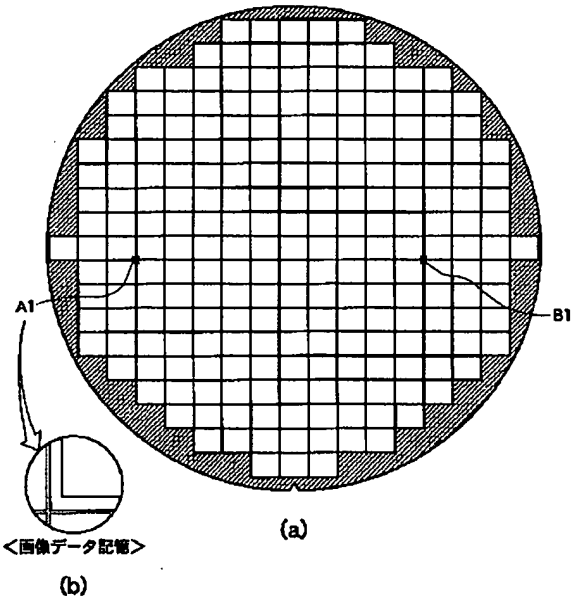
Drawing selection drawing 3



[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to semiconductor device manufacture, especially inspects the defect for every chip in a wafer process, and relates to the wafer coordinate recognition approach of automatic defective detection equipment of recognizing and detecting a rejected region.
[0002]
[Description of the Prior Art] A scanning electron microscope and the so-called SEM (Scanning Electron Microscope) are suitable for high scale-factor-ization of a sharp concavo-convex image. This SEM is applied and there is an image recognition technique called the review SEM (or INLINE-SEM) which performs step coverage of the interlayer insulation film on a wafer or wiring and observation of particle. Software is built with this review SEM and the automatic defective detection equipment which systematized automatic defective inspection is developed.
[0003] Automatic defective detection equipment advances defective inspection, while a suitable scale factor compares the field of each chip of next doors mutually optically to an inspected wafer first. That is, if abnormalities are accepted to the same field of the compared next chip, the defective coordinate data is acquired as a rejected region.
[0004] Next, alignment of this defective coordinate data and the inspected wafer is carried out, and a detailed defective review is performed by Review SEM. Defective detection of a wafer is automatically attained by finally offering the SEM image of a rejected region for the optimal scale factor.
[0005] Drawing 4 is a top view for explaining the alignment approach of the wafer in Review SEM applied to automatic defective detection equipment. In Review SEM, it points to A1 and B1 2 point as opposed to the inspected wafer WF (an operator may point and direct). The coordinate of each chip is searched for by count based on these points A1 and B1 (alignment coordinate acquisition). By such alignment coordinate, the data of the zero coordinate in each chip are also obtained.
[0006] The defective coordinate data of the inspected wafer inspected on the above-mentioned optical target is the information on the distance from a chip zero, and Review SEM moves to the part which defective coordinate data shows based on the above-mentioned alignment coordinate. Thereby, automatic defective detection equipment offers the SEM image of the actual abnormality part (rejected region) in an inspected wafer for the optimal scale factor to an operator.
[0007]
[Problem(s) to be Solved by the Invention] Thus, Review SEM uses the alignment coordinate acquired by count as mentioned above, and moves to the rejected region according to defective coordinate data. However, adjustment is not taken at all to distortion which generated the wafer coordinate determined by count like an alignment coordinate at the time of distortion by the inspected wafer itself, and exposure. Consequently, an error arises on a coordinate with each actual chip zero.
[0008] In the chip field near the periphery of a wafer, the error of an actual chip zero and

the chip zero on count becomes large especially. Thereby, when moving to a rejected region using an alignment coordinate, a highly competitive SEM image has a possibility that it may become impossible to catch a defect exactly.

[0009] This invention was made in consideration of the above-mentioned situation, the technical problem raises coordinate precision, and it is in offering the wafer coordinate recognition approach of automatic defective detection equipment that a highly competitive defective recognition image can be obtained exactly.

[0010]

[Means for Solving the Problem] The wafer coordinate recognition approach of the automatic defective detection equipment of this invention It is related with the automatic defective detection which extracts the actual rejected region in said inspected wafer as an image in Review SEM with reference to the defective coordinate data acquired from the inspected wafer. When coordinate data is set to said inspected wafer and an alignment coordinate is acquired, When memorizing the image data of the chip zero of arbitration and moving based on said alignment coordinate to the rejected region according to said defective coordinate data, It is characterized by correcting the error of said alignment coordinate by once moving to the zero coordinate of the chip which has a defect with reference to said defective coordinate data, and piling up with the image data of said chip zero.

[0011] According to the wafer coordinate recognition approach of this invention, in case it moves to a rejected region according to defective coordinate data, the error of an alignment coordinate is once corrected first. Since each defective coordinate data is the information on the distance from a chip zero with a defect, it is exactly movable to a rejected region with a sufficient precision from the chip zero by which the sector of calibration was carried out.

[0012]

[Embodiment of the Invention] Drawing 1 is a flow chart explaining the wafer coordinate recognition approach of the automatic defective detection equipment concerning the operation gestalt of this invention. At step 1, defective coordinate data is acquired from an inspected wafer. That is, defective inspection is advanced while a suitable scale factor compares the field of each chip of next doors mutually optically to an inspected wafer. That is, if abnormalities are accepted to the same field of the compared next chip, the defective coordinate data is acquired as a rejected region.

[0013] At step 2, the predetermined data which contain defective coordinate data in Review SEM (or called INLINE-SEM) are sent. Moreover, at step 3, coordinate data is set to an inspected wafer and an alignment coordinate is acquired. That is, as said drawing 4 explained, an alignment coordinate is acquired by count.

[0014] In this invention, in case an alignment coordinate is acquired in this step 3, the image data of the chip zero of arbitration is memorized. Since the image recognition of the angle of a predetermined chip is carried out from the first when setting up a coordinate, the image data is memorized. In addition, the above-mentioned step 2 and step 3 may interchange.

[0015] Next, at step 4, it once moves to the zero coordinate of the chip which has a defect with reference to the above-mentioned defective coordinate data. This is migration which uses an alignment coordinate, of course, and an error becomes greatly and small depending on a migration part.

[0016] Then, the image in the zero coordinate of an actual chip and the image data of the chip zero incorporated at the time of previous alignment coordinate acquisition are piled up, and the error of an alignment coordinate is corrected. That is, if the zero coordinate of an actual chip has shifted, the chip zero which is probably located in near is recognized and it is made to move slightly so that it may lap with the image data of the memorized chip zero. It is better for the superposition of this image to make a scale factor the same. For example, what is necessary is to adjust the scale factor of the image data of the chip zero incorporated at the time of previous alignment coordinate acquisition, and just to take adjustment.

[0017] Next, in step 5, it moves to the rejected region of the chip according to the above-mentioned defective coordinate data. Here, it is migration using the new alignment coordinate with which the error of a chip zero was corrected, and can move with a sufficient precision to a migration part exactly. Then, although not illustrated, the SEM image of the actual abnormality part (rejected region) in an inspected wafer is offered for the optimal scale factor.

[0018] That is, according to the wafer coordinate recognition approach of this invention, in case it moves to a rejected region according to defective coordinate data, the error of an alignment coordinate is once corrected first. Since each defective coordinate data is given for the information on the distance from a chip zero with a defect, it is exactly movable to a rejected region with a sufficient precision from the chip zero by which the sector of calibration was carried out. Consequently, a highly competitive SEM image can also catch a defect now exactly.

[0019] Drawing 2 (a) and (b) are the wafer top views showing more concretely the important section of the wafer coordinate recognition approach of the automatic defective detection equipment in drawing 1 , respectively. Drawing 2 (b) is the above-mentioned step 3, and shows memorizing the image data of the chip zero of arbitration to alignment coordinate acquisition and coincidence. That is, the points A1 and B1 for an alignment coordinate setup are first determined to the inspected wafer WF (drawing 2 (a)). At this time, for example, the predetermined field of the point A1, it memorizes as image data (drawing 2 (b)).

[0020] Drawing 3 is the expansion top view of the chip field in the inspected wafer WF in which the important section of the wafer coordinate recognition approach of the automatic defective detection equipment in drawing 1 is shown more concretely. Drawing expresses the above-mentioned step 4. First, with reference to defective coordinate data, it once moves to the zero coordinate (X1, Y1) by the alignment coordinate of Chip CHIP. The chip zero which laps with the image data of the previous point A1 is made to recognize by this, and the error of the chip zero of an alignment coordinate is corrected (chip zero coordinate (X2, Y2)).

[0021] it is like [according to superposition recognition of the above-mentioned image data, as for an alignment coordinate which is a wavy line, an error is corrected on count, and] a continuous line -- what -- it is mostly in agreement with an actual wafer coordinate. Thereby, it can move with a sufficient precision to a rejected region D exactly from a chip zero using defective coordinate data (arrow head 31).

[0022] Thus, according to the approach of the above-mentioned operation gestalt, in case it moves to a rejected region according to defective coordinate data, an error is corrected so that an actual inspected wafer may be suited in the alignment coordinate on count. The

adjustment over distortion by the inspected wafer itself and distortion generated at the time of exposure can be taken by this, and with high precision from the chip zero by which the sector of calibration was carried out, moreover, even if each defective coordinate data has a high scale factor, it is exactly movable to a rejected region.
[0023]
[Effect of the Invention] As explained above, in case it moves to a rejected region according to defective coordinate data according to this invention, the error of an alignment coordinate is once corrected first. Thereby, coordinate precision is raised and the wafer coordinate recognition approach of automatic defective detection equipment that a highly competitive defective recognition image can be obtained exactly can be offered.

[Translation done.]

TECHNICAL FIELD

[Field of the Invention] This invention relates to semiconductor device manufacture, especially inspects the defect for every chip in a wafer process, and relates to the wafer coordinate recognition approach of automatic defective detection equipment of recognizing and detecting a rejected region.

[Translation done.]

PRIOR ART

[Description of the Prior Art] A scanning electron microscope and the so-called SEM (Scanning Electron Microscope) are suitable for high scale-factor-ization of a sharp concavo-convex image. This SEM is applied and there is an image recognition technique called the review SEM (or INLINE-SEM) which performs step coverage of the interlayer insulation film on a wafer or wiring and observation of particle. Software is built with this review SEM and the automatic defective detection equipment which systematized automatic defective inspection is developed.
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[Translation done.]

EFFECT OF THE INVENTION

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[Translation done.]

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] Thus, Review SEM uses the alignment coordinate acquired by count as mentioned above, and moves to the rejected region according to defective coordinate data. However, adjustment is not taken at all to distortion which generated the wafer coordinate determined by count like an alignment coordinate at the time of distortion by the inspected wafer itself, and exposure. Consequently, an error arises on a coordinate with each actual chip zero.
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MEANS

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[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is drawing showing the flow chart explaining the wafer coordinate recognition approach of the automatic defective detection equipment concerning the operation gestalt of this invention.
[Drawing 2] (a) and (b) are the wafer top views showing more concretely the important section of the wafer coordinate recognition approach of the automatic defective detection equipment in drawing 1 , respectively.
[Drawing 3] It is the expansion top view of the chip field in the inspected wafer in which the important section of the wafer coordinate recognition approach of the automatic defective detection equipment in drawing 1 is shown more concretely.
[Drawing 4] It is a top view for explaining the alignment approach of the wafer in Review SEM applied to automatic defective detection equipment.
[Description of Notations]
1-5 -- Processing step
D -- Rejected region
CHIP -- Chip
WF -- Inspected wafer

[Translation done.]